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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,768	02/06/2002	Matthew S. Von Thun	02-0003 1496.00201	9287

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EXAMINER

LE, DINH THANH

ART UNIT PAPER NUMBER

2816

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary***(SUPPLEMENTAL)*

Application No.

10/068,768

Applicant(s)

THUN ET AL.

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 December 2002.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 and 7-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-18 & 20 is/are rejected.
- 7) ☒ Claim(s) 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☒ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_                      6) ☐ Other: \_\_\_\_\_

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**FINAL REJECTION (SPPLEMENTAL)**

***Response to Applicant's Amendment***

The rejections over Taguchi (US 6,225, 855), Okamura (US 5,712,536) and Akira (JP41120504) were withdrawn in view of the amendments to the claims.

***Claim Rejections***

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 3-4, 10, 11, 13 and 14, are rejected under 35 USC 102 (e) as being anticipated by Lien (US 6,441,651).

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Lien discloses in Figure 7 a source follower circuit (700) comprising a NMOS transistor (501) having a first gate (g) configured to receive an input voltage (Vin) of 5V and zero volt, a first drain (D) coupled to a first supply voltage (VCC) of 3.3V, a first resistive element (701) having a first side coupled to a first source (S) of the NMOS transistor (501) and a second side configured to receive a second voltage (VSS) of zero volt. Wherein the maximum voltage drop across a gate oxide of the first transistor (501) is equal to the difference between the Vin (5V) and the Vout (2V) at the output (212) or 3V (5V-2V) which does not exceed the difference between the first supply voltage of 3.3V and zero volt, see column 5, lines 20, 45.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 5, 7-9, 12, 15-18 and 20 are rejected under 35 USC 103 (a) as being unpatentable over Lien (US 6,441,651) in view of Ito et al (US 5,218,247).

Lien discloses in Figure 7 a source follower circuit (700) comprising all of the limitations of the claimed invention as discussed above but does not disclose that the input voltage ranges up to twice the first supply voltage with respect to the second supply voltage as recited in claim 2, the first device is a native NMOS device or a PMOS device as recited in claims 5, 7-8 and the first supply voltage is a ground voltage as recited in claim 9. Ito et al teaches a level shifter circuit (10) in Figure 3 comprising a PMOS transistor (13) coupled

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between a resistor (15) and ground for generating a first output voltage higher than or level shifted from the input voltage by a threshold voltage of the PMOS transistor, and a NMOS transistor (14) coupled between the resistor (16) and the VDD for generating a second output lower than or level shifted from the input voltage by the threshold voltage of the NMOS transistor. It would have been obvious to employ the PMOS transistor and the resistor taught by Ito et al in the circuit of Lien for the purpose of providing an output voltage higher than or level shifted from the input voltage by amount of the gate source voltage of the PMOS transistor.

Note that the MOS transistor having very low threshold voltage is well known in the art is and the input voltage of Lien is determined by the thickness of the gate oxide (threshold voltage) of the transistor (501). Selecting the native transistors for having very low threshold or the threshold voltage level of the transistor in the Lien reference to handle an input voltage twice the supply voltage for the purpose of accommodating with a particular environment or an application would have been obvious and considered to be a matter of design expedient for an engineer.

### ***Allowable Subject Matter***

Claim 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The claim would be allowable because the prior art does not disclose the multiplexer.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

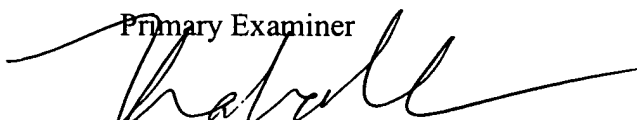
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dinh Le whose telephone number is (703) 305-3790. The examiner can normally be reached on Monday to Friday from 7:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7725.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

DINH LE  
Primary Examiner



May 13, 2003